

Abstracts

Design of a Novel FET Frequency Doubler Using a Harmonic Balance Algorithm

R. Gilmore. "Design of a Novel FET Frequency Doubler Using a Harmonic Balance Algorithm." 1986 MTT-S International Microwave Symposium Digest 86.1 (1986 [MWSYM]): 585-588.

The design of a wideband FET frequency doubler operating with a 4-8 GHz input bandwidth is described. The doubler and bandreject amplifier combination achieve an average conversion loss of 3.5 dB across the 8-16 GHz output band. The design method uses the harmonic balance algorithm implemented on an IBM PC-AT personal computer.

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